IN THE CLAIMS

The following shows the present status of all pending claims:

1. (Previously Presented) A semiconductor device having an input/output protection circuit section on a semiconductor substrate, the input/output protection circuit section comprising:

a plurality of field effect transistors connected in parallel, each of which has a source diffusion layer of a first conductive type and a drain diffusion layer of the first conductive type, and a gate electrode that is disposed between said source and drain diffusion layers;

a dopant diffusion region of a second conductive type that is set at a distance from said plurality of field effect transistors; and

an element isolation film located in the substrate between the dopant diffusion region of the second conductive type and the source diffusion layer of the first conductive type, for separating the dopant diffusion region from the source diffusion layer,

wherein said dopant diffusion region is connected to a reference potential,

wherein the drain diffusion layer is connected directly to an input/output terminal section without an intervening resistance element,

wherein a first conductive type well having a lower dopant concentration than the source diffusion layer is formed directly under the source diffusion layer and thereby the first conductive type well is electrically connected directly with the source diffusion layer, and

wherein the first conductive type well at least partially underlies the element isolation film.

2. (Previously Presented) The semiconductor device claimed in Claim 1, wherein said gate electrode, said source and drain diffusion layers of the first conductive type, and said dopant diffusion region of the second conductive type are disposed over a second conductive type well that is formed on the surface of the semiconductor substrate, and

wherein the bottom of said first conductive type well is formed at the same depth as the bottom of the second conductive type well or at a level deeper than the bottom of the second conductive type well.

3. (Previously Presented) The semiconductor device claimed in Claim 1, wherein said plurality of field effect transistors are N-channel type field effect transistors, and

wherein said source diffusion layer is also connected to the reference potential to which said dopant diffusion region is connected.

4. (Previously Presented) A semiconductor device having an input/output protection circuit section on a semiconductor substrate, the input/output protection circuit section comprising:

a complementary field effect transistor including a first field effect transistor having a source diffusion layer of a first conductive type, a drain diffusion layer of the first conductive type, and a gate electrode that is disposed between the source and drain diffusion layers of the first conductive type, and a second field effect transistor having a source diffusion layer of a second conductive type, a drain diffusion layer of the second conductive type, and a gate electrode that is disposed between the source and drain diffusion layers of the second conductive type,

wherein a first dopant diffusion region of the second conductive type is set at a distance from said first field effect transistor, and a second dopant diffusion region of the first conductive type is set at a distance from said second field effect transistor,

wherein at least an element isolation film is located in the substrate between the first dopant diffusion region of the second conductive type and the source diffusion layer of the first conductive type, for separating the first dopant diffusion regions from the source diffusion layer of said first field effect transistor,

wherein the first dopant diffusion region is connected to a first reference potential, and the second dopant diffusion region is connected to a second reference potential,

wherein the drain diffusion layer of the first field effect transistor and the drain diffusion layer of the second field effect transistor are each connected directly to an input/output terminal section without an intervening resistance element,

wherein a first conductive type well having a lower dopant concentration than the source diffusion layer of the first field effect transistor is formed directly under the source diffusion layer of the first field effect transistor and thereby the first conductive type well is

electrically connected directly with the source diffusion layer of the first filed effect transistor, and

wherein the first conductive type well of the first field transistor at least partially underlies the element isolation film of the first field effect transistor.

5. (Previously Presented) The semiconductor device claimed in Claim 4,

wherein the gate electrode, the source and drain diffusion layer of the first conductive type and the first dopant diffusion region of the second conductive type of the first field effect transistor are disposed over a second conductive type well that is formed on the surface of the semiconductor substrate, and

wherein the bottom of said first conductive type well of the first field effect transistor is formed at the same depth as the bottom of the second conductive type well of the first field effect transistor or at a level deeper than the bottom of the second conductive type well.

6. (Previously Presented) The semiconductor device claimed in Claim 5,

wherein, beneath the second conductive type well of the first field effect transistor, there is set a dopant high-concentration region containing second conductive type dopants with a higher dopant concentration than the second conductive type well of the first field effect transistor, and

wherein the bottom of said first conductive type well of the first field effect transistor is formed at the same depth as the bottom of said dopant high-concentration region or at a level deeper than the bottom of said dopant high-concentration region.

7. (Previously Presented) The semiconductor device claimed in Claim 4, wherein the first field effect transistor is an N-channel type field effect transistor, and

wherein the source diffusion layer of the first field effect transistor is also connected to the first reference potential, to which said first dopant diffusion region is connected.

8. (Previously Presented) A semiconductor device having an input/output protection circuit section on a semiconductor substrate, the input/output protection circuit section comprising:

a plurality of field effect transistors connected in parallel, each of which has a source diffusion layer of a first conductive type and a drain diffusion layer of the first conductive type and a gate electrode that is disposed between said source and drain diffusion layers;

a dopant diffusion region of a second conductive type that is set at a distance from said plurality of field effect transistors; and

an element isolation film located in the substrate between the dopant diffusion regions of the second conductive type and the source diffusion layer of the first conductive type, for separating the dopant diffusion regions from the source diffusion layer,

wherein said dopant diffusion region ity and said source diffusion layer of the first conductive type are connected to a reference potential,

wherein the drain diffusion layer is connected directly to an input/output terminal section without an intervening resistance element,

wherein a first conductive type well with a lower dopant concentration than the source diffusion layer is formed directly under the source diffusion layer and thereby the first conductive type well is electrically connected directly with the source diffusion layer, and

wherein the first conductive type well at least partially underlies an element isolation film separating the source diffusion area from the dopant diffusion region of the second conductive type.

9. (Previously Presented) A semiconductor device claimed in Claim 1, wherein the source diffusion layer is connected to the reference potential.

10. (Previously Presented) A semiconductor device claimed in Claim 1, wherein the source diffusion layer is connected to a ground terminal.